WHAT IS CLAIMED

1. A subscriber line interface circuit comprising:

a high voltage analog section, to which power sufficient for any signaling conditions of tip and ring conductors of a respective subscriber loop pair is supplied, and being operative to drive said tip and ring conductors of said respective subscriber loop pair in accordance with input signals supplied thereto; and

a low voltage digitally programmable signal generation and digital signal processing section, that is configured to monitor and program operational characteristics of, and supply said input signals to, said high voltage analog section.

2. The subscriber line interface circuit according to claim 1, wherein said high voltage analog section is configured to store operational control signals establishing multiple functional conditions of said high voltage analog section based upon requirements for a given mode of operation of said subscriber line interface circuit, as programmed into said low voltage digitally programmable signal generation and digital signal processing section.

3. The subscriber line interface circuit according to claim 1, wherein said high voltage analog section includes an input signal receiving unit, that is operative to interface and condition input voice and

ancillary signals, including low voltage signaling and ringing signals, supplied from said low voltage digitally programmable signal generation and digital signal processing section.

4. The subscriber line interface circuit according to claim 3, wherein said input signal receiving unit includes a voice signal path containing a voltage-sense, current-feed circuit to which voice signals are coupled from said low voltage digitally programmable signal generation and digital signal processing section, and a tip/ring amplifier unit, having respective tip and ring amplifier sections to which complementary polarity currents representative of voice signal signals are coupled from said voltage-sense, current-feed circuit, and having tip and ring outputs thereof adapted to be coupled to said tip and ring conductors of said respective subscriber loop pair.

5. The subscriber line interface circuit according to claim 4, wherein each of said tip and ring amplifier sections of said tip/ring amplifier unit is configured for multiple mode operation, and having gain characteristics which are programmable in accordance with the intended mode of operation of said subscriber line interface circuit, as controlled by said low voltage digitally programmable signal generation and digital signal processing section.

6. The subscriber line interface circuit according to claim 5, wherein said input signal receiving unit includes respective ancillary tip and ring signal paths containing respective tip and ring associated voltage-sense, current-feed circuits to which ancillary tip and ring signals are coupled from said low voltage digitally programmable signal generation and digital signal processing section.

7. The subscriber line interface circuit according to claim 6, wherein each of said tip and ring amplifier sections of said tip/ring amplifier unit is configured to operate at a first gain for voice signal transmission mode, and at a substantially increased second gain relative to said first gain for ancillary signal transmission mode.

8. The subscriber line interface circuit according to claim 7, wherein each of said tip and ring amplifier sections contains a plurality of front end transconductance circuits coupled to a shared operational amplifier gain section, and having feedback resistors coupled from an output of said gain section to inputs of respective ones of said plurality of front end transconductance circuits, that define respectively different gain characteristics with input resistors associated with drive signal currents from said input signal receiving unit.

9. The subscriber line interface circuit according to claim 8, wherein said plurality of front end transconductance circuits include a first front end transconductance circuit having a first valued feedback resistor coupled from said output of said gain section to a signal input of said first front end transconductance circuit, and a second front end transconductance circuit having a second valued feedback resistor, different from said first valued feedback resistor, and coupled from said output of said gain section to a signal input of said second front end transconductance circuit, and wherein said signal input of said first front end transconductance circuit is arranged to receive a selected one of said voice signals and low voltage ancillary signals, and wherein said signal input of said second front end transconductance circuit is arranged to receive a low voltage ringing signal.

10. The subscriber line interface circuit according to claim 9, wherein said first front end transconductance circuit is coupled to receive one of voice signals and low voltage signals, and said second front end transconductance circuit is coupled to receive ringing signals.

11. The subscriber line interface circuit according to claim 5, further including a battery bias unit coupled to selectively couple prescribed bias

voltages to voltage reference inputs of said tip and ring amplifier sections of said tip/ring amplifier unit in accordance with the mode of operation of said subscriber line interface circuit.

12. The subscriber line interface circuit according to claim 11, wherein said battery bias unit is coupled to a battery supply switch unit that is operative to provide for the selection from among a plurality of different battery voltages.

13. The subscriber line interface circuit according to claim 12, wherein said battery bias unit contains a set of switchable voltage divider networks coupled between said voltage reference inputs of said tip and ring amplifier sections of said tip/ring amplifier unit, and wherein said battery supply switch unit is operative to selectively couple either a high battery voltage VBH or a low battery voltage VBL to said battery bias unit.

14. The subscriber line interface circuit according to claim 13, further including a battery monitor unit coupled to provide said low voltage digitally programmable signal generation and digital signal processing section with an indication of the battery voltage being selectively coupled by said battery supply switch unit.

15. The subscriber line interface circuit according to claim 5, further including a sense amplifier coupled to outputs of said tip and ring amplifier sections of said tip/ring amplifier unit, and being operative to provide a voice signal summation for differential mode voice signals, and mutual cancellation of common mode signals.

16. The subscriber line interface circuit according to claim 15, wherein an output of said sense amplifier is adapted to be coupled through an auxiliary amplifier to an analog feedback monitor port for closing a loop to synthesize the output impedance of said subscriber line interface circuit.

17. The subscriber line interface circuit according to claim 15, wherein said sense amplifier comprises tip and ring associated voltage detectors, complementary-polarity coupled across tip and ring sense resistors at outputs of said tip and ring amplifier sections of said tip/ring amplifier unit.

18. The subscriber line interface circuit according to claim 5, wherein said tip and ring amplifier sections of said tip/ring amplifier unit are coupled to respective tip and ring path loop detectors, that provide outputs representative of sensed tip and ring currents for application to said low voltage digitally programmable signal generation and digital

signal processing section.

19. The subscriber line interface circuit according to claim 5, wherein said tip and ring amplifier sections of said tip/ring amplifier unit are operative to controllably limit transient current therein.

20. The subscriber line interface circuit according to claim 1, wherein said high voltage analog section includes a tip/ring amplifier unit having tip and ring outputs that are adapted to be coupled to respective ones of said tip and ring conductors of said respective subscriber loop pair, and having gain characteristics which are programmable in accordance with the intended mode of operation of said subscriber line interface circuit, as controlled by said low voltage digitally programmable signal generation and digital signal processing section.

21. The subscriber line interface circuit according to claim 20, wherein said input signal receiving unit includes respective ancillary tip and ring paths containing respective tip and ring associated voltage-sense, current-feed circuits, to which ancillary tip and ring control voltages are coupled from said low voltage digitally programmable signal generation and digital signal processing section, so as to place said tip/ring amplifier unit at respectively different gains

in association with respectively different modes of operation of said subscriber line interface circuit.

22. The subscriber line interface circuit according to claim 21, wherein said respective ancillary tip and ring paths and said tip/ring amplifier unit are configured to place said tip/ring amplifier unit at said respectively different gains in association with respectively different on-hook and off-hook modes of operation of said subscriber line interface circuit.

23. The subscriber line interface circuit according to claim 1, wherein said tip/ring amplifier is coupled to controllably supply said tip and ring conductors with respectively different sets of DC voltages, in accordance with the intended mode of operation of said subscriber line interface circuit, as controlled by said low voltage digitally programmable signal generation and digital signal processing section.

24. A high voltage analog circuit for a subscriber line interface circuit comprising:

an input signal receiving unit, that is operative to condition and interface input voice and low voltage signaling and ringing signals, supplied from a low voltage, digitally programmable signal generation and processing unit;

a multi-mode tip/ring amplifier unit, having tip and ring outputs thereof adapted to be coupled to tip

and ring conductors of a subscriber loop pair, and inputs coupled to receive and amplify said voice and low voltage signaling and ringing signals, in accordance with the mode of operation of said subscriber line interface circuit, and as conditioned and supplied thereto by said input signal receiving unit; and

a biasing unit, to which power for operating said high voltage analog circuit is coupled, and being operative to controllably couple prescribed bias voltages to said tip and ring amplifier sections of said tip/ring amplifier unit in accordance with the mode of operation of said subscriber line interface circuit.

25. The high voltage analog circuit according to claim 24, further including a control signal storage unit, which is operative to store control signals that establish operational characteristics of said high voltage analog section for a selected mode of operation of said subscriber line interface circuit, as supplied thereto from said low voltage, digitally programmable signal generation and processing unit.

26. The high voltage analog circuit according to claim 24, wherein said multi-mode tip/ring amplifier unit comprises tip and ring amplifier sections configured for multiple mode operation, and having gain characteristics which are programmable in accordance with the intended mode of operation of said subscriber line interface circuit, as controlled by said low

voltage, digitally programmable signal generation and processing unit.

27. The high voltage analog circuit according to claim 26, wherein each of said tip and ring amplifier sections contains a plurality of front end transconductance circuits coupled to a shared operational amplifier gain section, and having feedback resistors coupled from an output of said gain section to inputs of respective ones of said plurality of front end transconductance circuits, that define respectively different gain characteristics with input resistors associated with drive signal currents from said input signal receiving unit, and wherein one of said plurality of front end transconductance circuits is coupled to receive one of voice signals and low voltage signals, and another of said plurality of front end transconductance circuit is coupled to receive ringing signals.

28. The high voltage analog circuit according to claim 24, further including a sense amplifier coupled to outputs of said tip and ring amplifier sections of said dual mode tip/ring amplifier unit, and being operative to provide a voice signal summation for differential mode voice signals, and mutual cancellation of common mode signals.

29. The high voltage analog circuit according to claim 28, wherein an output of said sense amplifier is adapted to be coupled through an auxiliary amplifier to an analog feedback monitor port for closing a loop to synthesize the output impedance of said subscriber line interface circuit.

30. The high voltage analog circuit according to claim 28, wherein said sense amplifier comprises tip and ring associated voltage detectors, complementary-polarity coupled across tip and ring sense resistors at outputs of said tip and ring amplifier sections of said dual mode tip/ring amplifier unit.

31. The high voltage analog circuit according to claim 24, wherein said tip and ring amplifier sections of said dual mode tip/ring amplifier unit are operative to controllably limit transient current therein.

32. The high voltage analog circuit according to claim 24, wherein said tip and ring amplifier sections of said dual mode tip/ring amplifier unit are coupled to respective tip and ring path loop detectors, that provide outputs representative of sensed tip and ring currents for application to said low voltage, digitally programmable signal generation and processing unit.

33. The high voltage analog circuit according to claim 24, wherein said input signal receiving unit

includes respective ancillary tip and ring paths containing respective tip and ring associated voltage-sense, current-feed circuits, to which ancillary tip and ring control voltages are coupled from said low voltage, digitally programmable signal generation and processing unit, so as to place said multi-mode tip/ring amplifier unit at respectively different gains in association with respectively different modes of operation of said subscriber line interface circuit.

34. The high voltage analog circuit according to claim 33, wherein said respective ancillary tip and ring paths and said multi-mode tip/ring amplifier unit are configured to place said multi-mode tip/ring amplifier unit at said respectively different gains in association with respectively different on-hook and off-hook modes of operation of said subscriber line interface circuit.

35. The high voltage analog circuit according to claim 24, wherein said biasing unit is coupled to controllably cause said multi-mode tip/ring amplifier to supply said tip and ring conductors with respectively different sets of DC voltages, in accordance with the intended mode of operation of said subscriber line interface circuit, as controlled by said low voltage, digitally programmable signal generation and processing unit.